AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Original): A method of pipelined processing of a data packet (100,315) in a processing means (700) comprising at least two processing stages (205), said data packet (100) containing information, said method characterised by
associating (510) information reference (320; 325,330) to said data packet (315), said information reference (320; 325,330) comprising information relating to the length and position of the information contained in said data packet (315);
processing (520) said data packet (315) in a processing stage (205); and
if said processing (520) of said data packet (315) results in a change of the length or position of said information contained in said data packet (315), then altering (530) said information reference (320; 325,330) in order for said information reference (320; 325, 330) to reflect said change.

2. (Original): The method of claim 1, further comprising the step of: adding (505), prior to the step of associating (510), at least one bit (305, 310) to said data packet (100).

3. (Original): The method of claim 2, wherein said step of adding (505) comprises adding a header (305) and/or a tail (310) to said data packet (100).

4. (Currently Amended): The method of claim 1 ~~any one of the above claims~~, the method further comprising the steps of:
determining, upon the data packet exiting the last of said at least one processing stages, (540) whether any bits of the data packet (315) are superfluous; and, if any bits of the data packet (315) are superfluous, then
removing (545) said superfluous bits.

5. (Currently Amended): The method of claim 1 ~~any one of claims 1-3~~, the method further comprising the steps of: removing, upon the data packet exiting the last of said at least one processing stages, at least one bit from the data packet.

6. (Currently Amended): The method of claim 1 ~~any one of the above claims~~, wherein said information reference (320) is included in additional information (225) associated with said data packet.

7. (Currently Amended): The method of claim 1 ~~any one of the above claims~~, wherein prior to said step of processing (520) said data packet (315), said information reference (320) is stored in at least one register (230) accessible to the processing stage (205) performing said processing (520).

8. (Currently Amended): The method of claim 1 ~~any of the above claims~~, wherein said information reference comprises a length value (325) and an offset value (330), said length value (325) representing the length of the information contained in said data packet (315) and said offset value (330) indicating the position in said data packet (315) of the information contained in said data packet (315).

9. (Original): A processing means for pipelined processing of a data packet (100, 315), said processing means comprising at least one processing stage comprising a logic unit (210) and a register (220) for storing at least part of said data packet (100,315), said processing means being characterised in that
at least one register (230) for storing information reference (320) associated with said data packet (315) is accessible to said logic unit (210); and
at least one of at said at least one logic units (210) is adapted to operate upon said information reference (320).

10. (Original): The processing means of claim 9, further comprising means (715) for adding at least one bit to said data packet (1.00).

11. (Original): The processing means of claim 10, wherein said means (715) for adding comprises a buffer (720) and a shifter (725).

12. (Currently Amended): The processing means of claim 9 ~~any one of claims 9-11~~, the processing means further comprising means (730) for removing at least one bit from said data packet (315).

13. (Currently Amended): The processing means of claim 9 ~~any one of claims 9-12~~, wherein means (730) for removing comprises a shifter (735) and a buffer (740).

14. (Currently Amended): The processing means of claim 11 ~~or claim 13~~, wherein said shifter (725,735) is a barrel shifter.

15. (Currently Amended): The processing means (700) of claim 9 ~~any one of claims 9-14~~, wherein said at least one register (230) for storing information reference (230) is located in said processing stage (205).

16. (Currently Amended): The processing means (700) of claim 9 ~~any of claims 9-15~~, wherein said at least one register (230) for storing information reference comprises one register (230) for storing a length value (325) and another register (230) for storing an offset value (330).

17. (Original): An integrated circuit, characterised by a processing means (700) according to claim 9.

18. (Original): A computer unit characterised by an integrated circuit according to claim 9.